29.6 A 3MHz Low-Voltage Buck Converter with Improved Light Load Efficiency

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The synchronous buck switching converter has become ubiquitous in portable consumer electronics. However, one inherent disadvantage of this converter topology is its reliance on large, off-chip passive components. Although these components could be reduced in size by increasing the converter switching frequency, such a change would lead to reduced efficiency as a result of various converter losses that scale proportionally with switching frequency. This reduction is particularly severe at light loads.

For most low-voltage applications the dominant frequency-dependent loss at light loads is gate-drive loss. Pulse-frequency modulation (PFM) has been proposed as a means to scale such switching losses along with conduction losses to increase light-load efficiency [1]. The disadvantage of PFM is that it can generate spectral power-supply artifacts that degrade signal integrity in the load IC. Consequently, PFM operation is relegated to applications where only minimal IC functionality is required. In addition to PFM, resonant gate drive techniques have been proposed [2], but generally require components that are not easily integrated in standard CMOS processes.

We have previously described a method for scaling the gate swing of CMOS power devices to improve light-load efficiency [3]. Traditional PWM converters exhibit a rapid drop-off in efficiency as the load is decreased, an example of which is shown in [4]. The proposed gate-charge modulation (GCM) technique maintains near-constant efficiency over a broader dynamic load range by balancing the gate drive and channel conduction losses of the power MOSFETs. The underlying idea is similar in principle to the width-switching scheme described in [5]. In the current work, we develop a feedback control method for autonomous operation of GCM, as well as a gate charge recycling (GCR) technique that further improves efficiency. These techniques can be operated alone or in tandem.

Figure 29.6.1 shows a simplified top-level view of the buck converter. An external clock input, *CLK*, is fed into the pulse-width modulation (PWM) block to control the switching frequency while the duty-cycle is determined by the feedback control signal, V_{con}. The PWM block generates two non-overlapping gate drive signals, PWM_p and PWM_n, with dead-time T_{dead} to ensure that the two power devices do not conduct simultaneously. These signals in turn drive their respective gate drivers. The PWM block also generates a clock signal, PWM_{samp}, whose rising and falling edges are aligned with the midpoint of the PWM ON and OFF times. This signal is used to sample the drain-source voltages of the power devices when $I_D = I_{load}$, required for the GCM controller described below.

Figure 29.6.2 shows a simplified schematic of the charge modulated gate driver with feedback control for the NMOS power device. The driver for the PMOS device is similar. At light loads, the RMS channel current, I_{rms}, is dominated by the ripple component of the inductor current, Δi, leading to an optimal gate swing that is approximately independent of load current, and given by

$$V_{swing,opt} \approx \sqrt{\frac{D_{sw}\Delta i^2}{3kC_{gate}V_{in}f_{sw}}} + |V_{th}|. \qquad (1)$$

Here, D_{sw} is the fraction of switching cycle during which the power device conducts, k is a process-dependent parameter, and V_{th} is the device threshold voltage. As I_{load} increases, I_{rms} is increasingly affected by the DC component of the current. In this region, forcing the drain-source voltage of the power devices to a constant (given in Fig. 29.6.2 as $V_{ds,ref}$), achieves near-optimum efficiency.

The circuit of Figure 29.6.2 operates as follows: the drain-source voltage of M_1 is sensed while the device is conducting. As mentioned before, PWM_{samp} ensures that V_{ds} is sampled when $I_D = I_{load}$, an assumption made in the derivation of the V_{ds} reference value. These samples are compared to $V_{ds,ref}$ and the feedback controller acts to minimize the resulting error. A lower bound is placed on V_{con} by the voltage limiter block, setting a minimum gate swing that is equal to $V_{swing,opt}$. Assuming that the gate of M_1 is initially discharged, a falling *PWM* edge causes the gate of M_2 to be pulsed low, with V_{con} setting the length of the on-time, T_{pulse}. Turning M_2 on pulls the gate of M_1 up to a value, V_{swing} " V_{in}, set by the feedback controller. To turn M_1 off, a *PWM* rising edge turns M_3 on, pulling V_{g1} to ground.

The GCR circuit used to drive the NMOS power device is illustrated in Fig. 29.6.3. The overshoot of the underdamped network comprising L_{store}, C_{store} and the parasitic series resistance modeled by R_{par}, is exploited to enhance charge storage over what is possible with purely capacitive charge-sharing. Assume that the gate of M_1 is initially charged to V_{in}, that C_{store} is initially discharged, and that M_2 and M_3 are off. While Φ_1 is pulsed for T_{store} seconds, M_4 and M_5 conduct and transfer charge through L_{store} to C_{store}. Φ_1 ideally goes low when V_{store} reaches its peak value in order to reuse the maximum amount of charge possible. Φ_3 then goes high to turn M_1 off completely. To turn M_1 back on, Φ_3 goes low and Φ_1 is pulsed once again, returning a portion of the stored charged to the gate of M_1. M_2 subsequently turns on to bring the gate of M_1 to V_{in} and M_6 is turned on to prepare the storage network for the following cycle. To combine GCR with GCM, M_2 is simply pulsed for a short time, swinging the gate of M_1 to the desired level as described previously.

For the present design, both NMOS and PMOS drivers use L_{store} = 22nH, while C_{store} is 35pF and 85pF for the NMOS and PMOS networks, respectively. The GCR system was tested using both on-chip and off-chip passive components. In order to reduce potential timing errors when generating T_{store}, a calibration step that seeks to maximize the return charge is included in the system operation. For this design, GCR performance was limited by a larger-than-expected series parasitic resistance in the storage network.

Figure 29.6.6 shows key performance data for the converter when both gate charge modulation and recycling (GCMR) are enabled. Figure 29.6.4 shows a plot of measured efficiency versus load current with and without GCMR gate drive enabled. For V_{out} = 1.8V the converter achieves a peak efficiency of 89.1% at I_{load} = 125mA. The efficiency remains above 80% over a 20:1 load current range spanning from 20mA to I_{max} = 400mA. The plot of Figure 29.6.5 shows the reduction in power loss versus I_{load} when the GCMR drivers are enabled. At 20mA, P_{loss} is reduced by 22.7%, from 11.5mW to 8.9mW. At 200mA the reduction is 8.7%. A micrograph of the test die, fabricated in a 0.5µm CMOS n-well process, is shown in Fig. 29.6.7.

Acknowledgements:
The authors would like to thank National Semiconductor for funding this work and for fabricating the test chip, Prof. Boris Murmann for helpful feedback on the manuscript, and Dr. Ömer Oralkan for providing the die micrograph.

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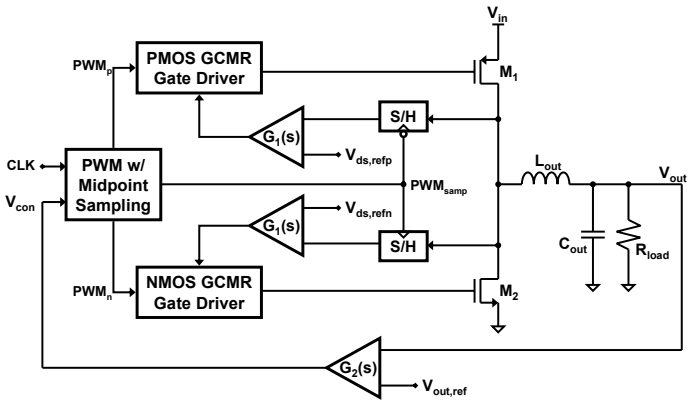

Figure 29.6.1: Top-level schematic of low-voltage DC-DC step-down converter with GCMR gate drivers.

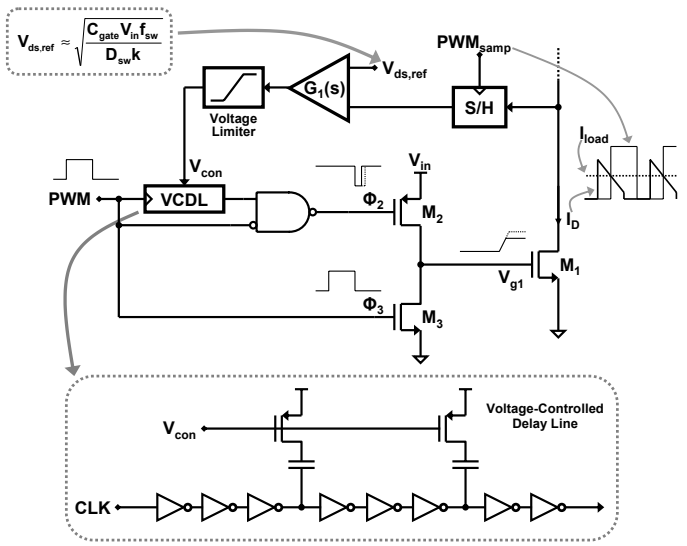

Figure 29.6.2: Schematic of the GCM driver.

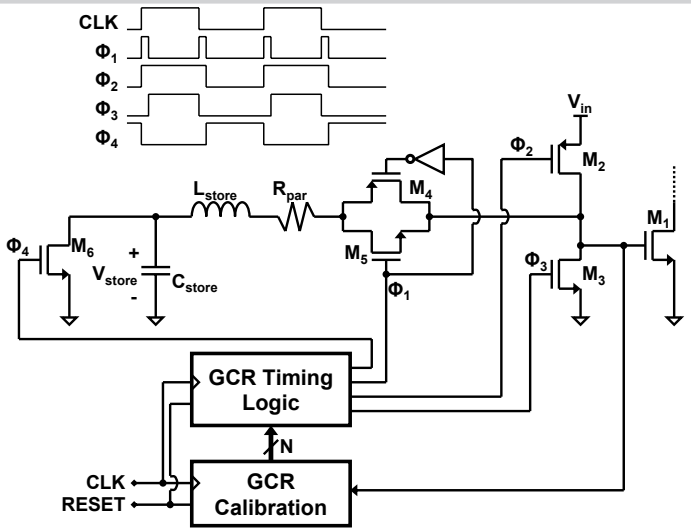

Figure 29.6.3: Schematic of the GCR driver and illustration of clock, switch, and gate signals.

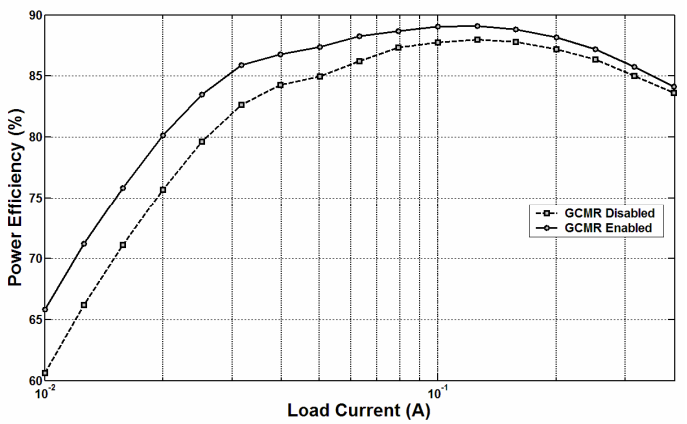

Figure 29.6.4: Measured conversion efficiency for V_{out} = 1.8V with and without GCMR gate drive enabled.

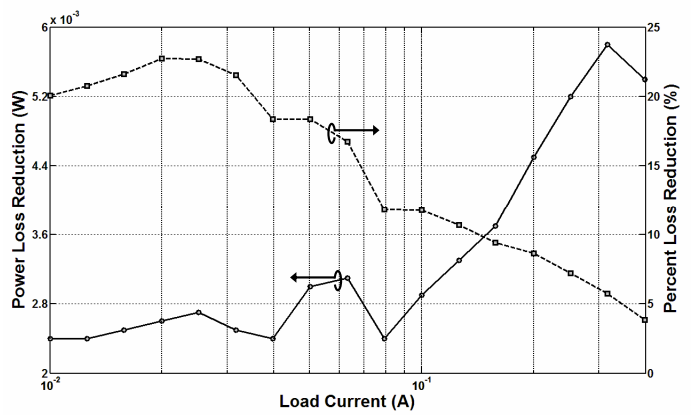

Figure 29.6.5: Measured power loss reduction (V_{out} = 1.8V) when GCMR gate drive is enabled.

Performance Summary

Device Parameter	Value		
Input Voltage, V_{in}	3.6V		
Switching Frequency, f_{sw}	3MHz		
NMOS Device Width, W_n	21mm		
PMOS Device Width, W_p	60mm		
Output Inductance, L_{out}	3.3µH		
Output Capacitance, C_{out}	4.7µF		
Chip Area	5.3mm²		
Process	0.5µm CMOS, 5AL, 2PS		
Output Voltage, V_{out}	1V	1.5V	1.8V
Peak Efficiency, η_{peak}	81.8%	88.0%	89.1%
Efficiency @ 20mA (Rail-to-Rail)	66.7%	72.5%	75.7%
Efficiency @ 20mA (GCMR)	70.5%	76.7%	80.1%
P_{loss} Reduction @ 20mA	16.2%	19.8%	22.7%
P_{loss} Reduction @ 100mA	8.7%	12.6%	11.8%

Figure 29.6.6: Performance summary.

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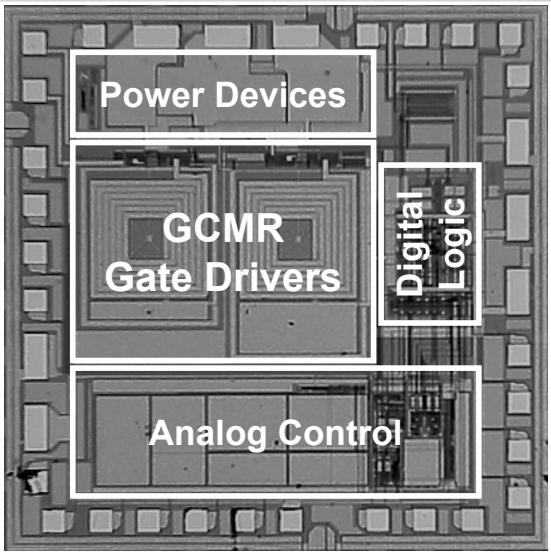

Figure 29.6.7: Die micrograph.

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